REMARKS/ARGUMENTS

1.) Claim Amendments

Claims 11-20 are pending in the application. The Applicant has amended claims 15 and 20. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

2.) Information Disclosure Statement

The information disclosure statement filed 06/25/2004 was objected to because legible copies of the foreign patents and other prior art was missing. The applicant now resubmits the information disclosure statement filed 06/25/2004 along with another copy of the foreign patents and other prior art listed.

3.) Claim Rejections – 35 U.S.C. § 112

Claims 15 and 20 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter as the invention. The Examiner stated the relationship between the different factors listed in claims 15 and 20 is not defined. The Applicant has amended claims 15 and 20 to define the relationship between the listed factors. Basis for the amendments is found in the specification on page 7, line 23 through page 8, line 21; and on page 11, line 21 through page 12, line 27. Therefore, the withdrawal of the § 112 rejection is respectfully requested.

4.) Claim Rejections – 35 U.S.C. § 103 (a)

Claims 11-12, 14, and 17-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McHarg, *et al.* (US 5,291,482) in view of Acharya (US 7,110,359). The Applicant contends that McHarg does not disclose or suggest the claimed limitations asserted by the Examiner. Regarding independent claims 11 and 17, the Applicant notes the following regarding the Examiner's citations in McHarg.

McHarg teaches one buffer between the write bus and read bus. The claimed invention teaches one buffer between the input line and the TDM bus, and one buffer

between the TDM bus and the output line. In other words, McHarg's buffer is a centralized component. In the claimed invention, the TDM bus is a centralized component (see Figure 1). This is an essential difference because the TDM bus is a passive component (PCB backplane), and a central active switch component such as McHarg's buffer is not needed. This reduces the chance of having a "single point of failure" in the system, because there are no centralized active components like a buffer in the claimed invention.

McHarg relates to a packet switch, while the claimed invention relates to a time division multiplexed (TDM)-based switch, which leads to several basic differences in the way the switches operate. McHarg teaches that the packet receiver dynamically requests pointers from a buffer manager (Col. 6, lines 9-11) whenever an incoming packet arrives. This is typically for a packet switch, which uses different pointers for a given input line each time a packet is received. The claimed invention uses the same pointer for a given input line each time (... by means of respective pointers allocating one memory area in a data buffer for each of the input lines), and does so only when the scheduler determines it is time to move data from the input buffer.

Furthermore, McHarg teaches that a pointer is distributed to the packet receiver where it is used to calculate an address that is sent over the write-bus to the buffer where the address is used as a write address for incoming data. The claimed invention does not operate in this manner. Since the pointer for each input line does not change and always points to the same address, the claimed invention does not transport a calculated buffer address over the TDM bus.

McHarg teaches that a timer is used for determining whether a pointer is encountered within a certain time period. This has no relation to the function of the timer recited in the Applicant's independent claims 11 and 17. The timer recited in claims 11 and 17 has no relation to the pointers mentioned in the same claim. The timer for each input line is used to indicate the time at which data transfer requests for the respective input line are to occur. McHarg does not teach anything about timers for requesting data from the input lines, because McHarq transfers packets to the buffer immediately upon arrival. (Abstract; and Col. 2, lines 51-56).

The Examiner notes that McHarg does not teach a FIFO buffer for each input line or the use of a scheduler. In paragraph 9, the Examiner asserts it would have been obvious to a person of ordinary skill in the art to use Acharya's FIFO buffers and scheduler in McHarg's packet switch to control access to the memory. The Applicant respectfully disagrees.

The combination of McHarg and Acharya is technically improper because the combination is not operable. In a packet switch as disclosed by McHarg, the packets are transferred to the buffer immediately upon arrival. Therefore, the addition of the scheduler from Acharya is meaningless and would not be considered by one of ordinary skill in the art.

For all the above reasons, the Applicant contends that a *prima facie* case of obviousness has not been established. Therefore, the withdrawal of the § 103 rejection and the allowance of independent claims 11 and 17 are respectfully requested.

Dependent claims 12, 14, 18, and 19 recite additional limitations in combination with the novel and unobvious elements of claims 11 and 17. Therefore, their allowance is also respectfully requested.

With regards to claims 12 and 18, the Applicant reiterates that McHarg teaches that the packet receiver dynamically requests pointers from a buffer manager (Col. 6, lines 9-11) when an incoming packet arrives. This is typically for a packet switch, which uses different pointers for a given input line each time a packet is received. The claimed invention uses the same pointer for a given input line each time (... by means of respective pointers allocating one memory area in a data buffer for each of the input lines).

With regards to claims 14 and 19, the Applicant reiterates that a packet switch as disclosed by McHarg transfers each packet to the buffer immediately upon arrival. Therefore, the addition of the scheduler from Acharya is meaningless and would not be considered by one of ordinary skill in the art.

In paragraph 12, the Examiner asserts it would have been obvious to a person of ordinary skill in the art to use Acharya's weighted round-robin scheduling mechanism with the McHarg packet switch to cure an overflow condition. The Applicant respectfully

notes that the round robin scheduler in the claimed invention is used to share a common buffer by the input sources, not to cure an overflow condition, so this argument is not relevant.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over McHarg, *et al.* (US 5,291,482) in view of Acharya (US 7,110,359) and further in view of Reid (US 4,131,762). The Examiner contends that McHarg and Acharya show the claimed invention regarding the lookup table except for a counter synchronized to a clock, which is shown by Reid. The Applicant respectfully disagrees.

The lookup table in McHarg maps from a logical destination contained in the routing byte in the received packet to a physical channel number. (Col. 6, lines 22-27). This is typical for a packet-switched system. The connection table in the claimed invention, on the other hand, maps a data byte in the data buffer to a timeslot on the TDM bus (indicated by the timeslot counter). Mapping a data byte to a TDM timeslot is totally different from mapping a logical destination to a physical destination. Thus, a connection table with the claimed functionality is not taught or suggested by the combination of McHarg, Acharya, and Reid. Therefore, the allowance of claim 13 is respectfully requested.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over McHarg, *et al.* (US 5,291,482) in view of Acharya (US 7,110,359) and further in view of Sanders, *et al.* (US 6,931,022). The Examiner cited Sanders for allegedly showing frames being transmitted through the time slot buses either in a minimum delay modus or a constant delay modus. The Applicant respectfully disagrees.

A constant delay timeslot allocation scheme requires buffering of one additional TDM frame before data is sent out on the TDM bus to have full flexibility of timeslot allocation on the TDM bus. McHarg does not describe this additional buffer in the packet receiver. It is not likely that McHarg can transfer the time-slots over the write bus in an order other than the order in which they arrived on the input line, as recited in Applicant's claim 16, because this requires a connection table that can map each

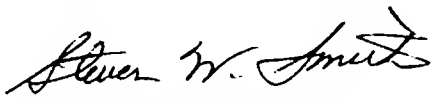
timeslot on the input to a timeslot on the bus. Thus, it is not obvious that McHarg can use a constant delay timeslot allocation scheme. Therefore, the allowance of claim 16 is respectfully requested.

5.) Conclusion

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for claims 11-20.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would expedite the prosecution of the Application.

Respectfully submitted,



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